REMARKS

Claims 1-15 and 21-25 are pending in the application.

Applicant notes with appreciation the withdrawal of the previous rejection.

Applicant notes with appreciation the acceptance of the drawings.

Claims 1-15 and 21-25 have been rejected in the Office Action to which the present Reply is responsive. Applicant respectfully traverses these rejections. Based on the present Reply, Applicant respectfully requests reconsideration and withdrawal of the rejections of Applicant's claims, and passage of the present application to allowance and issue.

REJECTIONS OVER HATTORI ET AL. IN VIEW OF MORI ET AL.

In the Office Action, claims 1-15 and 21-25 were rejected under 35 U.S.C. § 103(a) as obvious over Hattori et al. (U.S. Patent 6,252,294) in view of Mori et al. (U.S. Patent 5,162,241). The Examiner asserted that Hattori teaches various elements of the claimed invention, but admitted that Hattori et al. fails to teach all the features of the claimed invention. The Examiner cited and relied upon Mori et al. in order to remedy the admitted deficiencies of Hattori et al. Applicant respectfully traverses the rejections over Hattori et al. in view of Mori et al. for the following reasons.

1. The Combined References Fail to Disclose All the Limitations of Applicant's Claims.

With respect to claim 1, the Examiner asserted that Hattori et al. teaches a process including a step of:

> forming at least one gettering plug in each cavity 6, each gettering plug comprising doped fill material 7 containing a plurality of gettering sites wherein the doped fill material is polysilicon formed by LPCVD deposition of the polysilicon and a dopant in the cavity (See col. 5, lines 66-67):

The Examiner made similar assertions with respect to claims 9 and 21, specifically asserting the presence of a dopant in the polysilicon gettering plug.

Applicant respectfully traverses the Examiner's assertions, since Hattori et al. fails to disclose or suggest that the polysilicon in the gettering plugs is doped. The disclosure at col. 5, lines 66-67, cited by the Examiner apparently in support of these assertions, states only:

> After formation of the grooves 6, a polycrystalline silicon film 7 is deposited on the groove 6 through CVD.

At no time does Hattori et al. disclose that the polysilicon is doped. Polysilicon is disclosed by Hattori et al. as the gettering material for embodiment 2 at col. 7, lines 26-27, for embodiment 3 at col. 10, lines 29-30, for embodiment 4 at col. 11, lines 43-44, and for embodiment 5 at col. 13, lines 18-19. There is no disclosure or any suggestion whatsoever by Hattori et al. that the polysilicon could or should be doped. Hattori et al. suggests silicon oxide as a possible alternative gettering material, but silicon oxide is not doped polysilicon, as would be recognized by any person of ordinary skill in the art.

Thus, Hattori et al. fails to disclose or suggest, and fails to provide any motivation whatsoever for, substitution of doped polysilicon for the gettering material. The disclosure of Mori et al. fails to provide any suggestion that a doped material could be placed in a plug or trench as in Hattori et al.

For the foregoing reason alone, the combination of Hattori et al. and Mori et al. fails to disclose all the limitations of Applicant's claimed invention, as described in claims 1, 9 and 21. Therefore, the rejection should be withdrawn for this reason alone. Applicant respectfully requests the withdrawal of all rejections based on Hattori et al.

2. There is No Motivation for the Asserted Combination.

The Examiner admitted that Hattori et al. fails to teach subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites wherein the gettering step gettered impurities migrate into a silicon substrate layer below the dielectric insulation layer.

The Examiner attempted to remedy this admitted failing by citing Mori et al. However, Mori et al. does not relate to SOI semiconductor devices, but relates to the very old use of bulk silicon substrates, in which a gettering layer is applied to the backside of the substrate. The reliance on Mori et al. is faulty for several reasons. Applicant respectfully submits that the asserted combination of Mori et al. and Hattori et al. fail to render obvious Applicant's invention, as described in claims 1, 9 and 21, and the claims dependent thereon, and requests the withdrawal of the rejections thereover.

First, the asserted combination of Hattori et al. and Mori et al. is faulty because Hattori et al. clearly teaches away from the method employed by Mori et al. At col. 1, lines 29-37, Hattori et al. describes the type of gettering disclosed by Mori et al. At col. 1, lines 44-55, Hattori et al. describes attempts to combine the method of Mori et al. with SOI devices, and states that such is not effective since the impurities have insufficient energy to reach the gettering layer. The various other methods discussed by Hattori et al. from col. 1, line 56 to col. 2, line 34, all of which involve some combination of the Mori et al. method with SOI devices, are also disclosed as unsatisfactory. Thus, no person of ordinary skill in the art, would be motivated to seek to combine Mori et al. with Hattori et al., based on the teaching away from such combination in Hattori et al. Indeed, Applicant respectfully submits that no person of ordinary skill would attempt to combine the teachings of Mori et al. with any SOI device, at least for the reasons set forth in Hattori et al. For this reason, the combination of Hattori et al. and Mori et al. fails to provide even a *prima facie* case of obviousness of the presently disclosed and claimed invention, as described in claims 1, 9 and 21.

Second, as noted by the Examiner in citing Mori et al., at col. 2, lines 32-37, Mori et al. discloses that impurities are gettered into the gettering layer, and requires that the gettering layer

be removed. There is nothing in Hattori et al. which suggests or requires that the gettering material be removed. In fact, any person of ordinary skill in the art would readily recognize that it would be impractical or impracticable to remove the gettering material from either the structure of Hattori et al. or from the Applicant's claimed invention. There is no suggestion in Mori et al. that the step of removing the gettering layer from the wafer could be omitted. In fact, Mori et al. clearly requires and claims that the contaminated layer of the gettering site in which the contaminant impurities are trapped is removed, to prevent migration of the gettered impurities back into the silicon. For this additional reason, the combination of Hattori et al. and Mori et al. would not have lead a person of ordinary skill in the art to Applicant's invention. If these two references were combined, Applicant's claimed invention would not be obtained, and a person would not be lead to the claimed invention by the combination. For this further reason, the combination of Hattori et al. and Mori et al. fails to provide even a *prima facie* case of obviousness of the presently disclosed and claimed invention, as described in claims 1, 9 and 21.

Third, if a person of ordinary skill attempted to combine the teachings of Hattori et al. with the teachings of Mori et al., the person would obtain one of the embodiments discussed in the background of the Hattori et al. reference, which plainly are different from the presently claimed invention. Thus, for this additional reason, the combination of Hattori et al. and Mori et al. fails to provide even a *prima facie* case of obviousness of the presently disclosed and claimed invention, as described in claims 1, 9 and 21.

3. The Dependent Claims Include Additional Distinguishing Features.

With respect to claims 8, 15 and 22, while Mori et al. discloses subjecting the semiconductor wafer to conditions to getter at least one impurity into a silicon substrate layer, it is a distortion of the Mori et al. teaching to equate this to the gettering step of Applicant's claimed invention. Mori et al. clearly and indisputably requires that in the gettering, the impurities pass through the substrate and thence into the gettering layer, which is subsequently removed, leaving an uncontaminated substrate behind. There are specific teachings throughout

Mori et al. that the impurities should be removed from and not allowed to return to the substrate. This is fully distinct from the presently claimed invention of claims 8, 15 and 22, which recite that the impurities migrate into a silicon substrate ~~layer below the dielectric insulation layer~~. Furthermore, since Mori et al. is not an SOI device, it has no dielectric insulation layer, so the impurities cannot be left there. Thus, for this additional reason, the combination of Hattori et al. and Mori et al. fails to provide even a *prima facie* case of obviousness of the presently disclosed and claimed invention, as described in claims 8, 15 and 22.

In addition, the dependent claims include additional features which, when taken together with the foregoing claims, further define Applicant's invention over the disclosures of Hattori et al. and Mori et al., in combination. For example, Hattori et al. fails to disclose or suggest the use of LPCVD as recited in claim 2. While Hattori et al. discloses CVD, it fails to disclose or suggest LPCVD. As admitted by the Examiner, neither Hattori et al. nor Mori et al. disclose or suggest the claimed dopants, recited in claims 3, 4, 10 and 25. Neither reference discloses a gettering plug in which the fill material is polysilicon and a dopant, in which the dopant is added by one of codeposition or implantation, as recited in claim 12, or by implantation as recited in claim 21 (which is, of course not a dependent claim).

Applicant respectfully submits that for at least the foregoing reasons, Hattori et al. in combination with Mori et al. fails to disclose or suggest Applicant's presently claimed invention. Accordingly, Applicant respectfully requests the Examiner to reconsider and withdraw the rejection of Applicant's claims over the prior art, and to indicate that the claims are allowable. Applicant respectfully requests notice to such effect.

Applicant respectfully submits that all of the presently pending claims 1-15 and 21-25 are allowable over the art of record for the foregoing reasons.

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CONCLUSION

For the foregoing reasons, Applicant respectfully requests the Examiner to reconsider and withdraw the rejections of Applicant's claims, and to allow the presently pending claims. Notice of Allowance is respectfully requested.

In the event issues remain in the prosecution of this application, Applicants request that the Examiner telephone the undersigned attorney to expedite allowance of the application. Should a Petition for Extension of Time be necessary for the present Reply to the outstanding Office action to be timely filed (or if such a petition has been made and an additional extension is necessary) petition therefor is hereby made and, if any additional fees are required for the filing of this paper, the Commissioner is authorized to charge those fees to Deposit Account #18-0988, Docket No. F0556.

Respectfully submitted,

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